# On the design of an FPGA-Based OFDM modulator for IEEE 802.16-2004

Joaquín García, René Cumplido
*Department of Computer Science, INAOE, Puebla, Mexico*
*joaquingr@ccc.inaoep.mx, rcumplido@inaoep.mx*

## Abstract

*Current and future communication schemes tend to use OFDM systems in order to provide high baud rates and less inter symbol interference. Some examples are 802.11, 802.16, MC-CDMA, Digital Video Broadcasting, Wireless USB and Wireless Firewire. Trying to provide a solution to the new emerging devices, slow standard adoption and poor spectrum use, Joe Mitola introduced the concept of "Software Defined Radio" (SDR), which involves exhaustive configurable digital signal processing like FFT. This work presents the design, validation and FPGA based implementation of an "Orthogonal Frequency Division Multiplexing" (OFDM) modulator for IEEE 802.16 using a high level design tool, and also reports the resources requirements for the presented system.*

**Keywords:** *OFDM, FPGA, 802.16, SDR, 4G*

## 1. Introduction

Orthogonal Frequency Division Multiplexing (OFDM) could be tracked to 1950's, but it had become very popular at these days, allowing high speeds at wireless communications [1]. OFDM could be considered either a modulation or multiplexing technique, and its hierarchy corresponds to the physical and medium access layer. A basic OFDM system consists of a QAM or PSK modulator/demodulator, a serial to parallel / parallel to serial converter, and an IFFT/FFT module. The iterative nature of the FFT and its computational order makes OFDM ideal for a dedicated architecture outside or parallel to the main processor. Using FPGA instead of an ASIC gives also flexibility for reconfiguration, which is a need for the Software Defined Radio (SDR) concept. The focus of this work is to validate the suitability of reconfigurable devices such as FPGAs to perform "Intermediate Frequency" (IF) processing to support SDR [2]. This work presents the mapper, interleaver, IFFT and prefix adding modules for a Std. 802.16 compliant OFDM modulator implemented on FPGA using a high-level design tool.

Present work is divided as follows: Section II presents the related work; section III presents a brief description of the Std. IEEE 802.16 and OFDM fundamentals; at section IV the block diagram and the explanation of each block as the system design are presented; section V is dedicated to results and finally at section VI conclusions are presented.

## 2. Related Work

This section presents relevant previous works related to OFDM implementations for IEEE 802 standards. Moises Serra [3] shows the design of an OFDM transmitter as part of an OFDM demonstrator for Hiperlan/2. The features of that transmitter are: 36 Mbit/s, ¾ punctured code rate, 16QAM, 64-IFFT and cyclic prefix of 16 samples, meanwhile this work presents all the QAM and PSK alphabets supported by the Std. IEEE 802.11a [4] and 802.16a [7]. This work stores normalized values for modulation tables, while Serra's work multiplies for a fixed value to normalize. Other interesting and contrasting work is presented by Ma. José Canet [5] showing implementation issues of a digital transmitter for an OFDM with optimized VHDL against System Generator results. Canet's work is focused on solutions for the OFDM signal generation in base-band and IF.

Chris Dick [6] emphasizes the suitability of high-level design tools when designing sophisticated systems, and the importance to design FPGA systems rather than ASIC for accomplishing one day the SDR "Software Defined Radio" concept and give a high-level overview of the FPGA implementation, that work emphasizes the synchronization, packet detection, preamble correlator, channel estimation and equalization; that is mainly at the OFDM receiver for the 802.11.

Proceedings of the 2005 International Conference on Reconfigurable Computing and FPGAs (ReConFig 2005)
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## 3. 802.16 and OFDM Overview

### 3.1. OFDM Fundamentals

OFDM is a special case of multi-carrier transmission, where a single data stream is transmitted over a number of lower rate sub-carriers. On classical frequency division multiplexing the total band is divided into N non-overlapping frequency channels, while on OFDM the band is divided into a number of overlapping frequency channels [8] but with orthogonal frequencies, the consequence is a better use of the available spectrum. Those orthogonal frequencies are obtained by using the IFFT. An OFDM symbol is formed by the sum of N orthogonal frequency signals, and then to avoid inter-symbol interference, a guard time greater than the expected delay is added, during that time the signals are replicated on a cyclic prefix, as Fig. 1 shows, in order to prevent the effect of selective frequency delay.

As described at Std. IEEE 802.16 [7], the OFDM Physical layer (PHY) transmitter blocks are: FEC Coder, Interleaving/Mapping, IFFT, Guard Interval (Cyclic Prefix), In Phase and Quadrature Modulation (IF) and finally the RF modulation. Those blocks as specified by IEEE 802.16 are shown at Fig. 2.

### 3.2. The standard 802.16

Std. 802.16 specifies OFDM as the multiplexing and modulation technique for the fixed broadband wireless access supporting this standard, which covers the physical and medium access specifications.

Some of the specified aspects of the standard are IFFT/FFT of 256 or 2048 points, depending on the use of OFDM or OFDMA. For the case of OFDM (256 points FFT) 200 sub-carriers are used for data pilots from a QPSK, 16-QAM or 64-QAM alphabet; there

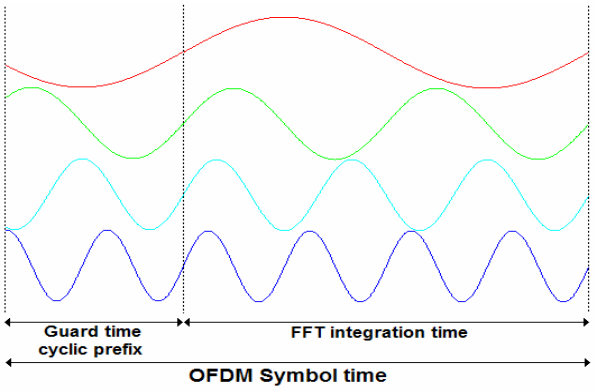


Fig. 1. OFDM Symbol.

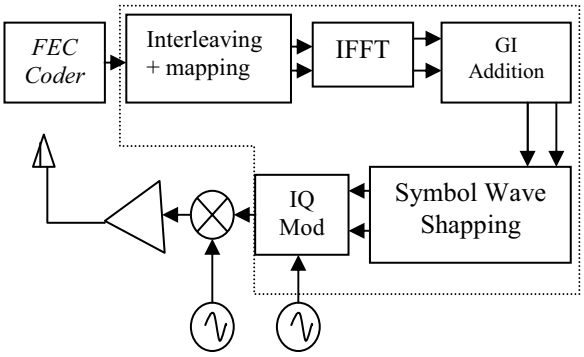


Fig. 2. 802.16 Transmitter block diagram for the OFDM PHY.

are 8 pilots at specific indexes, the other 56 points are zero padded. After IFFT module, a cyclic prefix is added to have a complete OFDM symbol, the number of points for the prefix is variable and could be 1/4, 1/8, 1/16 or 1/32 depending on the bandwidth (BW) employed; for the Std. 802.16 many BW could be used from 1.5 to 28 MHz and must be multiple of 1.25, 1.5, 1.75, 2.0 or 2.75 MHz, thus the OFDM symbol duration can be from 8 to 125 μs. This work is presented using an OFDM scheme (256 points FFT), with a BW of 20 MHz and a prefix of 64 points that is a 1/4 of the 256, having a 320 points symbol.

## 4. System Design Flow

Xilinx System Generator, which runs over MatLab Simulink, was used on this work. This tool allows a high level abstraction of the system. Not only the design was performed using System Generator but verification and finally targeting to a specific FPGA.

This work divides the design into functional subsystems: PSK or QAM mapping, pilot generator, inter-leaver which mixes all sources (mapped data, pilots and zero pads), IFFT and prefix adding. Regarding the frequency of operation, this design uses an 80 MHz for the main clock which is down-sampled to obtain a 16 MHz, used before IFFT block and 20 MHz after IFFT block. All blocks use a 10-bit signed fixed point representation but IFFT that uses 16-bit resolution.

### 4.1. PSK or QAM mapping

This block consist of a number of ROMs containing the constellation mapping for each of the specified modulation schemes (QPSK, 16-QAM and 64-QAM), two multiplexers which select the In Phase and Quadrature data from the desired modulation scheme

stored on ROMs. Finally data are stored on a FIFO component to pass to next stage, as shown at Fig. 3.

### 4.2. Inter-leaver

Inter-leaver block combines data, pilots and zero pads. The structure for the IFFT input must be {28 zeros, 100 data, zero, 100 data, 27 zeros}, pilots are included on data and their indexes corresponds to -88, -63, -38, -13, 13, 38, 63, 88. The complete sequence indexes goes from -128 to +127. The function of this block is to interleave data, pilots and zeros as described by the mentioned structure. For this purpose a counter is used to know which input turn is, then using combinational logic, a multiplexer is selected to take data, pilot or zero according to its position given by the counter. This model is shown at Fig. 4.

### 4.3. IFFT & Prefix adding

Parallel butterfly algorithms for IFFT are the most suitable for OFDM [9], this work uses a radix-4 butterfly generated by the Xilinx IP core Generator. Data arrives to IFFT module at 16 MHz, but it works three times slower than the main clock which was set at 80 MHz, for this reason the incoming data is up-sampled by 5 and then down-sampled by 3, thus additional logic is required to mark the data as valid or not, and then pass it to the IFFT block.

The IFFT block takes 768 cycles to perform the transform (256 times 3), the results are stored into four FIFO blocks; two of them store the real and imaginary coefficients of the 256 points transform; the other two FIFO stores the last 64 real and imaginary coefficients that will be used as cyclic prefix, in order to have an 320 points symbol at the end. The architecture of this module is shown at Fig. 5.

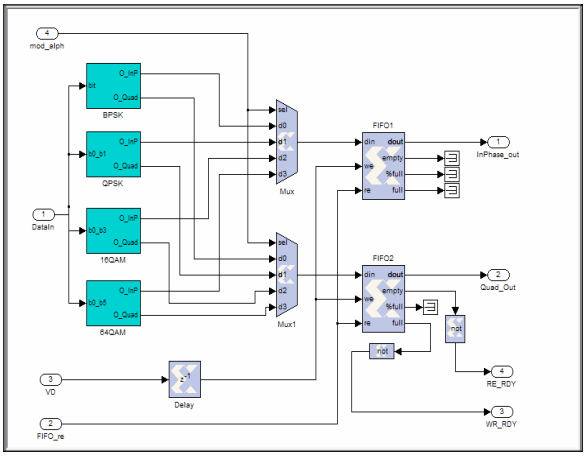


Fig. 3. PSK or QAM mapping model.

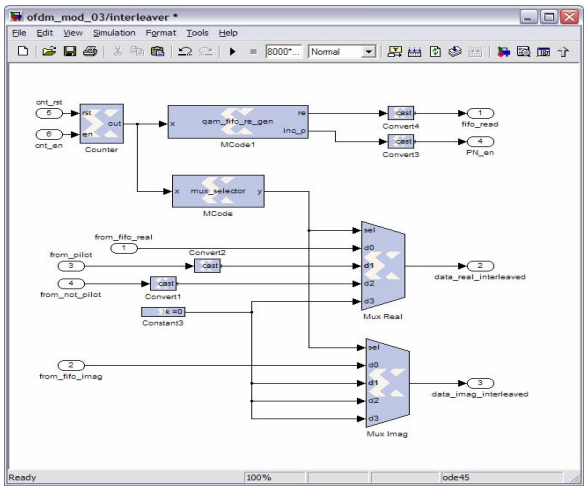


Fig. 4. Inter-leaver model.

## 5. Results

The conformance with Sdt 802.16 [7] could be validated by running a simulation at MatLab using test data provided by the standard. Using this high level tool simplifies all prototyping process contrasting with a VHDL based testbench validation approach which would require more prototyping time and effort. All specified modulation schemes (QPSK, 16-QAM and 64-QAM) were tested at base band frequency (20 MHz), no channel model were used, neither DDS or DDC were performed at this time.

The model was targeted to a Virtex 2 xc2v3000-4fg676, the result was that all mentioned modules requires around 18% of the available resources, while the Maximum Frequency estimated was 98.376 MHz, which is enough for the requirement of 80 MHz architecture to generate 20 MHz (OFDM Symbol frequency specified at 802.11a) and 16 MHz clocks. Detailed area results are shown at Tables 1. These results were obtained using Xilinx´s ISE 6.3i tool.

Since this work implements 802.16, it needs more resources than the presented at similar works for 802.11. Contrasting 802.11 needs 64 points FFT while 802.16 needs at least 256 points FFT. Now if it is considered that 802.11 takes around 12% of the same device, It can be said that a device similar to the Virtex 2 xc2v3000-4fg676, could be configured either as 802.11 or 802.16 modulator.

Since 802.16 implementations are not reported, it is helpful to compare some modules with similar works, for instance, this work IFFT takes 768 cycles to perform the transform while the ASIC DSP proposed at [10] would take 2056. The results from the IFFT are buffered to a dual port memory at [5], this work uses a FIFO structure to store results and cyclic prefix which is a simple way to produce the prefix adding stage.

Mentioned related works use fixed configuration of the system to be implemented, this work supports all possible QAM or PSK alphabets. This work has been tested with a ¼ cyclic prefix, but it could be switched to any other supported size.

One of the limitations found while working with System Generator was the use of only one main clock, besides this inconvenient this tool allows a rapid prototyping

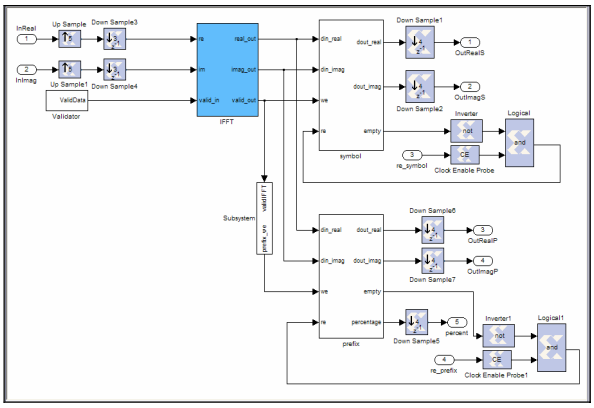


Fig. 5. IFFT and prefix adding model.

TABLE I
AREA RESULTS

| Area metrics for a XC2V3000-4FG676 device | | |
|---|---|---|
| **Parameter** | **Used** | **%** |
| Number of Slices | 2614 | 18 |
| Number of Slice Flip Flops | 3566 | 12 |
| Number of 4 input LUTs | 4304 | 15 |
| Number of bonded IOBs | 29 | 5 |
| Number of BRAMs | 12 | 12 |
| Number of GCLKs | 1 | 6 |

## 6. Conclusion

It has been presented the complete design, validation and implementation of an OFDM modulator compliant with the Std. IEEE 802.16. This work was performed using System Generator and MatLab & Simulink. The results presented show that it is possible to implement an OFDM modulator for IEEE Std. 802.16 using a current medium density device like Virtex II. These results show that current devices could support the SDR concept at IF processing level even at high arithmetic demanding standards or process. This work also presents the required resources to implement the Std. 802.16 on a Virtex II device.

Future work includes adding the FEC module, demodulator modeling as well other standards like MC-CDMA. The final goal is to encapsulate many standards into one configurable architecture to support SDR and 4G.

## Acknowledgments

This work has been partially supported by CONACyT "National Council for Science and Technology" of México under grant number 181689.

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